REMARKS

No new matter has been added. The Applicants request entry of the foregoing amendment prior to examination of the application on the merits.

Respectfully submitted,

Joseph A. Walkowski
Registration No. 28,765
Attorney for Applicants
TRASKBRITT
P. O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: (801) 532-1922

Date: November 13, 2001

JAW/df/dlm
N:\2269\2869.7\PRELIMIN.AMD

APPENDIX A

Version with markings to show changes made

IN THE SPECIFICATION:

Please replace paragraph **[0001]** with the following:

[0001] This application is a continuation of application Serial No. 09/652,274, filed August 31, 2000, [pending] now U.S. Patent 6,274,390 B1, issued August 14, 2001, which is a continuation of application Serial No. 09/443,080, filed November 18, 1999, now U.S. Patent 6,215,181 B1, issued April 10, 2001, which is a continuation of application Serial No. 08/728,302, filed October 8, 1996, now U.S. Patent 6,008,538, issued December 28, 1999.

IN THE CLAIMS:

1. (Amended) A memory module, comprising:

a substrate;

at least two sites on said substrate, each of [the] said at least two sites having mounted thereon a memory chip with substantially the same memory capacity, said memory chips providing a memory capacity for said memory module; and

at least one other site on said substrate for mounting at least one additional memory chip thereon, [the] said at least one additional memory chip having a functional memory less than [the] said memory capacity of said memory module.

2. (Amended) A memory module, comprising:

a substrate;

at least two sites on said substrate, each of [the] said at least two sites having mounted thereon a memory chip with substantially the same memory capacity, said memory chips providing a memory capacity for said memory module; and

at least one other site on said substrate configured to accept either of at least two other memory chips of different [size] sizes.

3. (Amended) A memory module, comprising:

a substrate having a plurality of memory chips mounted thereon; and

a programmable device adapted to reroute input and output paths to and from said plurality of memory chips to bypass [non-functional] nonfunctional memory in at least one of said plurality of memory chips, extending to one or more additional locations on said substrate and configured to incorporate functional memory of one or more additional chips disposed at said one or more additional locations on said substrate into said rerouted input and output paths.

4. (Amended) The memory module of claim 3, further comprising at least one additional memory chip mounted on at least one of said additional locations, operably coupled to said programmable device and providing functional memory in an amount equivalent to or greater than [the] said [non-functional] nonfunctional memory.

5. (Amended) The memory module of claim 4, wherein said at least one additional memory chip contains at least some [non-functional] nonfunctional memory.

6. (Amended) The memory module of claim 4, wherein said at least one additional memory chip comprises at least two memory chips having different memory capacity and being placed at different additional locations.

7. (Amended) The memory module of claim 3, wherein said programmable device comprises a traffic-control EEPROM.

8. (Amended) A memory module comprising:

a plurality of chips mounted to a substrate, said plurality of chips collectively exhibiting an amount of [non-functional] nonfunctional memory exceeding a memory capacity of any one chip of said plurality; and

at least one additional memory chip providing an amount of functional memory equal to or greater than said amount of [non-functional] nonfunctional memory.